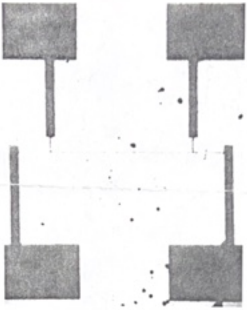
Miniaturisation at Glasgow

The microcomputer chip, carrying data on wires no larger than one fiftieth of the diameter of a human hair, has become a symbol of '80s technology. The components on which it relies, however, were invented half a century ago, yet they continue to function despite the dramatic miniaturisation required to pack tens of thousands of them into a square centimetre of silicon 'real estate'.

It is unlikely that the process of miniaturisation can be carried much further without accompanying changes in device behaviour. The physical processes on which field effect transistors, bipolar transistors and diodes rely set fundamental limits to the validity of accepted device theory. A transistor whose features are smaller than the mean free path of the current carriers or the separation between dopant atoms, or comparable with the wavelength of the electron, is unlikely to behave in a classical manner. These effects will not be significant, however, until device structure reaches 10-100nm in size which is well beyond the capabilities of even the most advanced photolithography. Research being carried out by the authors' group at Glasgow University's Department of Electronic and Electrical Engineering is developing lithographic techniques suitable for 10nm dimensions which it is hoped will allow size dependent effects to be probed.

The two viable candidates for very high resolution pattern definition are electron beam lithography and soft x-ray contact printing. Both have been examined in detail by the Glasgow group. The first of these, electron beam lithography, involves drawing the pattern in an electron-sensitive material with a focused electron probe. The sensitive layer, or resist, is usually a polymer and is coated on to the substrate to be patterned. Poly(methyl methacrylate) (PMMA) has the highest resolution of any polymeric resist. While the electron probe may be focused down to atomic dimensions the ultimate resolution of the pattern is determined by electron scattering in both the resist and the substrate. If resist and substrate are both thin, so that relatively few scattering events occur as the electron passes through them, then pattern linewidths approach the 10nm target with centre-to-centre spacings of 40-50nm. These limits appear to be determined by the range of secondary electrons generated during resist exposure and by the size of the polymer molecule.



A 40nm-wide gold-palladium 4-point probe test structure for low temperature electron localisation studies. The wire is approximately 25 microns long.

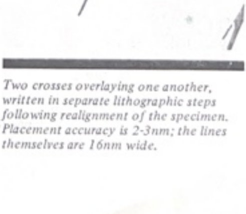
A typical resolution test pattern in 5nm thick platinum palladium alloy. Lines are 16nm wide and minimum centre-to-centre spacing is 53nm. Single layer PMMA resist, 50kV, 8nm electron beam.

Multi-layer resists

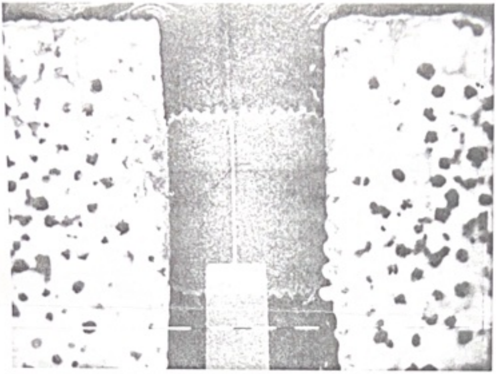
A thin resist layer cannot stencil deep patterns, so the requirement of very high resolution competes, for example, with the need for thick metal tracks to minimise electrical resistance. Some benefit can be obtained by using multi-layer resists. The system most used by the Glasgow group consists of two layers of PMMA differing slightly in sensitivity. This increases the aspect ratio (line width to line height) by a factor of two or so. Moreover, lift-off processing, in which the developed resist stencil is first overcoated with metal and then dissolved away, becomes much more reliable with this technique. Further improvements in aspect ratio require resists with greater mechanical strength and higher softening temperatures than PMMA-type polymers and this usually makes processing more complicated. We have experimented with silver-doped arsenic trisulphide glass overcoating polyimide as a possible solution to the problem. The glass is rendered insoluble in alkaline solutions when the electron beam drives silver from a thin top coating into the glass on exposure. The glass pattern then masks the underlying polyimide in an oxygen-reactive ion-etching step. Aspect ratios of 4:1 can be obained, testifying to the strength of polyimide, but resolution is disappointing. Despite hopes that the resolution of the apparently amorphous glass would not be determined by molecular size, there would appear to be sufficient structure in the glass to impose a 30nm linewidth limit.

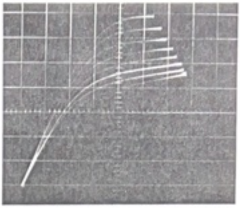
Very high resolution

The thin substrate requirement of very high resolution is another problem for the device engineer. Although some materials can be fabricated in thin-film form, it is not possible to do so for all materials of interest. We have shown, however, that 20nm lines can be written even on solid substrates and that, provided great precision is used in setting resist exposure, close-packed structures can be resolved in spite of the interactions which arise through scattering. We have also experimented with very soft (280eV) x-rays to replicate electron beam written masks on to solid substrates. While this technique has adequate ultimate resolution for this purpose, the effects of diffraction through the resist, the difficulties of making high contrast masks



Two crosses overlaying one another, written in separate lithographic steps following realignment of the specimen. Placement accuracy is 2-3nm; the lines themselves are 16nm wide.





Left: Scanning electron micrograph of a 75nm gate length GaAs MESFET written entirely by electron beam techniques. The gate is made of aluminium; source and drain contacts are of gold-germanium alloy.
Above: DC characteristics of the 75nm gate length MESFET.

by the e-beam step and the fragility of masks of adequate x-ray transparency all reduce resolution and conspire against the practicality of this approach. We believe that certain specialised applications can benefit from x-ray printing at the 0.1 micron level, but the flexibility of e-beam lithography confers a superiority which alternative techniques will find difficult to surpass. It remains true that the ultimate ultra-small structure is best fabricated on thin substrates and we expect to obtain our most interesting small device results using this approach.

Lithographic achievements

To put our lithographic achievements in perspective, state-of-the-art integrated circuit technology uses 1 micron minimum linewidths, so our structures are 100X smaller. The scope for investigating the effects of further miniaturisation is enormous and is of obvious significance to industry. In association with Plessey, RSRE and British Telecom we have started to fabricate FET structures in the 10nm to 1 micron gate length range. The smallest devices will be made on GaAs membranes, but development devices have already been tested on solid GaAs and Si substrates. Both GaAs and Si device technologies present interesting spatial resolution problems beyond the initial lithography. In silicon, for example, less than 100nm might separate implanted areas of material, and this separation must be preserved during the annealing step required to activate the implant. In GaAs, ohmic contacts to the source and drain on the FET are made by sintering Au-Ge-Ni alloys which are highly mobile. Novel heat treatment techniques will be needed to maintain sub-0.1 micron gaps in both these cases. Nevertheless, we have made workable 0.1 micron gate length Si MOSFETs and 0.075 micron gate length GaAs MESFETs, have measured their dc characteristics and are now considering how best to test these devices, whose switching speeds could well be less than 10ps.

Unique patttern writer

Yield is a major consideration when embarking upon a programme of device assessments. To date, all our patterns have been written with a converted Philips scanning electron microscope working at 50kV with an 8nm diameter electron probe. This instrument is capable of writing very few devices per day, all of which can be rendered useless by process failures or by a few minutes' careless testing. SERC funds will allow us to purchase a unique pattern writer operating at up to 100kV and forming 2nm diameter probes. This will be equipped with a high capacity stage to give us much greater throughput. The grant will also support the programme of device research and further development of lithographic techniques.

High-speed devices might well exhibit effects arising from the lack of carrier scattering events and the wave-nature of the electron. These will be most marked in the finest structures. Physicists have already begun to look for these phenomena, for example, in very narrow straight wires made by edge-shadowing techniques. Here the versatility of very high-resolution electron beam lithography comes into its own. One can, for example, test the electronic behaviour not only of straight wires, but also of very sharp (<10nm radius) bends and repeated meanders. One can look for evidence of ballistic transport between close-spaced electrons on semiconductor substrates.

A joint programme of research in these areas will soon commence between ourselves and Drs Lawrence Eaves and Peter Maine of the Department of Physics, Nottingham University, supported by an SERC grant. A further grant will finance an exploratory study of the positioning of biological material on patterned surfaces. This research will be undertaken jointly between ourselves and Professor Adam Curtis of the Cell Biology Department of Glasgow University.

Enormous scope

The scope for research arising from the development of ultra-small patterning techniques is enormous. Minimum linewidths amount to about 20 gold atoms. Positional accuracy is approximately 5 or 6 atoms. Coupled with advance deposition techniques such as Molecular Beam Epitaxy, materials can now be structured in three dimensions with almost atomic precision. What phenomena will the engineering community turn to its advantage with such unprecedented machining technology?

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